Solution

Sub:- Electronic Devices
B-Tech IIIrd sem, ECE

Section - 'A'

(i) b → Diffusion Current

(ii) b → Si is more thermally stable

(iii) $2V_m$

(iv) large

(v) True

(vi) b → I_{CO}

(vii) a → $-\frac{2I_{DSS}}{V_p}\left[1-\frac{V_{GS}}{V_p}\right]$

(viii) b → It is faster

(ix) c → Relaxation oscillator

(x) a → Depends upon Junction temp. & forward current.

$$\therefore \quad \sigma_n = q N_D \mu_n$$

$$\therefore \quad 28.571 = 1.6 \times 10^{-19} \times N_D \times 1500 \times 10^{-4}$$

$$\therefore \quad N_D = 1.190 \times 10^{21} \text{ per m}^3$$

and $n_i = 1.45 \times 10^{16}$ per cm^3

$$= \frac{1.45 \times 10^{10}}{10^{-6}} \text{ per m}^3$$

$$= 1.45 \times 10^{16} \text{ per m}^3$$

Now height of potential barrier means junction potential V_J.

$$\therefore \quad V_J = V_T \, ln \left[\frac{N_A N_D}{n_i^2} \right]$$

At room temperature, $V_T = 26 \text{ mV} = 26 \times 10^{-3}$ V

$$V_J = 26 \times 10^{-3} \times ln \left[\frac{1.315 \times 10^{21} \times 1.19 \times 10^{21}}{(1.45 \times 10^{16})^2} \right]$$

$$\therefore \quad V_J = 0.591 \text{ V.}$$

Q-2(a) ~~Ex. 1.20~~ : *The resistivity of the two sides of a step graded germanium junctions are 5 Ω-cm on p-side and 2.5 Ω-cm on n-side. Calculate the height of the potential barrier. If the resistivities of the sides are interchanged, calculate the height of the potential barrier.* **(Dec-91)**

Assume : $\mu_n = 0.38 \, m^2/V\text{-}s$, $n_i = 2.5 \times 10^{13}$ per cm^3, $\mu_p = 0.18 \, cm^2/V\text{-}s$

Sol. : Case i] $\rho_p = 5 \, \Omega\text{-cm} = 5 \times 10^{-2} \, \Omega\text{-m}$

$$\therefore \quad \sigma_p = \frac{1}{\rho_p} = \frac{1}{5 \times 10^{-2}} = 20 \, (\Omega\text{-m})^{-1}$$

Now for p-type material, $p_p \cong N_A$

$$\therefore \quad \sigma_p = q N_A \mu_p$$

$$\therefore \quad 20 = 1.6 \times 10^{-19} \times N_A \times 0.18$$

$$\therefore \quad N_A = 6.95 \times 10^{20} \text{ per m}^3$$

Similarly $\rho_n = 2.5 \, \Omega\text{-cm} = 2.5 \times 10^{-2} \, \Omega\text{-m}$

$$\therefore \quad \sigma_n = \frac{1}{\rho_n} = \frac{1}{2.5 \times 10^{-2}}$$

$$= 40 \, (\Omega\text{-m})^{-1}$$

Now for n-type material, $n_n \cong N_D$

$$\therefore \quad \sigma_n = q N_D \mu_n$$

$$\therefore \quad 40 = 1.6 \times 10^{-19} \times N_D \times 0.38$$

$$\therefore \quad N_D = 6.578 \times 10^{20} \text{ per m}^3$$

$$n_i = 2.5 \times 10^{13} \text{ per cm}^3 = \frac{2.5 \times 10^{13}}{10^{-6}} \text{ per m}^3$$

$$= 2.5 \times 10^{19} \text{ per m}^3$$

Now $V_T = 26$ mV at room temperature.

$$\therefore \quad V_J = V_T \, ln\left[\frac{N_A N_D}{n_i^2}\right]$$

$$= 26 \times 10^{-3} \, ln\left[\frac{6.95 \times 10^{20} \times 6.58 \times 10^{20}}{(2.5 \times 10^{19})^2}\right]$$

$$= 0.171 \text{ V.}$$

Case ii]

$$\rho_n = 5 \times 10^{-2} \; \Omega\text{-m}$$

$$\therefore \quad \sigma_n = \frac{1}{\rho_n} = 20 \; (\Omega\text{-m})^{-1}$$

and

$$\sigma_n = q N_D \mu_n$$

$$\therefore \quad 20 = 1.6 \times 10^{-19} \times N_D \times 0.38$$

$$\therefore \quad N_D = 3.28 \times 10^{20} \text{ per m}^3$$

while

$$\rho_p = 2.5 \; \Omega\text{-cm} = 2.5 \times 10^{-2} \; \Omega\text{-m}$$

$$\therefore \quad \sigma_p = \frac{1}{\rho_p} = 40 \; (\Omega\text{-m})^{-1}$$

and

$$\sigma_p = q N_A \mu_p$$

$$\therefore \quad 40 = 1.6 \times 10^{-19} \times N_A \times 0.18$$

$$\therefore \quad N_A = 1.389 \times 10^{21} \text{ per m}^3$$

$$V_T = 26 \times 10^{-3} \text{ V}$$

$$\therefore \quad V_J = V_T \, ln\left[\frac{N_A N_D}{n_i^2}\right]$$

$$= 26 \times 10^{-3} \, ln\left[\frac{1.389 \times 10^{21} \times 3.28 \times 10^{10}}{(2.5 \times 10^{19})^2}\right]$$

$$= 0.171 \text{ V.}$$

And the current equation (2.15) is applicable for both forward and reverse biased conditions and completely describes the V-I characteristics of p-n junction diode. The sign of voltage V must be considered appropriately for applying the equation in case of forward and reverse biased conditions.

2.6.2 Mathematical Expression for the Dynamic Resistance

We have seen earlier that the dynamic resistance is the reciprocal of the slope of the V-I characteristic of a diode. For the incremental changes in voltage and current we can write,

$$r = \frac{1}{\text{Slope of graph}}$$

$$= \frac{1}{\left[\frac{dI}{dV}\right]} \quad \ldots (2.18)$$

Now current equation of a diode is given by,

$$I = I_0 \left(e^{V/\eta V_T} - 1\right)$$

$$\therefore \quad \frac{dI}{dV} = I_0 \left[\frac{1}{\eta V_T} \cdot e^{V/\eta V_T}\right]$$

$$\therefore \quad \frac{dI}{dV} = \frac{I_0 e^{V/\eta V_T}}{\eta V_T} \quad \ldots (2.19)$$

$$\therefore \quad r = \frac{1}{\left[\frac{dI}{dV}\right]}$$

$$= \frac{\eta V_T}{I_0 e^{V/\eta V_T}} \quad \ldots (2.20)$$

But from the current equation we can write,

$$I = I_0 e^{V/\eta V_T} - I_0$$

$$\therefore \quad I_0 e^{V/\eta V_T} = I + I_0 \quad \ldots (2.21)$$

Substituting in equation (2.20), we get,

$$r = \frac{\eta V_T}{I + I_0} = \text{Dynamic resistance} \quad \ldots (2.22)$$

While determining the value of dynamic resistance under forward biased and reverse biased conditions, the general expression, equation (2.20) is used. For forward biased condition treat V positive while for reverse biased condition treat V as negative, while using the expression. The following example will clear the use of the generalised expression in calculating forward and reverse dynamic resistance.

2.8.1 Mathematical Expression of Transition Capacitance C_T

Consider a p-n junction diode, the two sides of which are not equally doped. Impurity added on one side is more than the other. Assume that p-side is lightly doped and n-side is heavily doped. As depletion region penetrates lightly doped side, the most of depletion region is on p-side as it is lightly doped as shown in the Fig. 2.15.

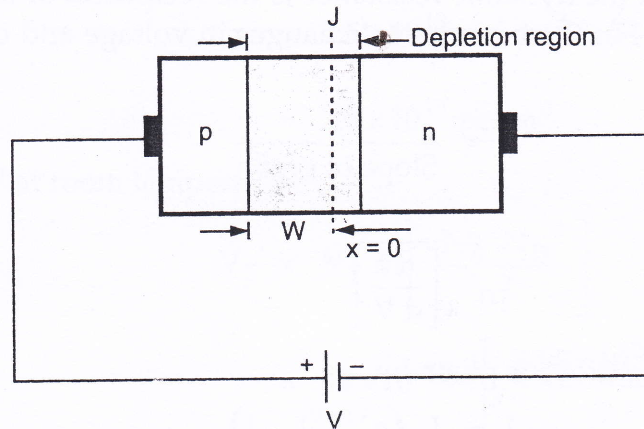


Fig. 2.15 Unequally doped p-n junction diode

It can be further assumed that concentration of acceptor impurity on p-side (N_A) is much less than the concentration of donor impurity on n-side (N_D). Hence the width of depletion region on n-side is negligibly small compared to width of depletion region on p-side. Hence the entire depletion region can be assumed to be on the p-side only.

The relationship between potential and charge density is given by Poisson's equation as,

$$\frac{d^2 V}{d x^2} = \frac{q N_A}{\varepsilon} \quad \text{... (2.36)}$$

where x = the distance measured from the junction.

and ε = the permittivity of the semiconductor.

$$\varepsilon = \varepsilon_0 \varepsilon_r \quad \text{... (2.37)}$$

where ε_0 = permittivity of free space

$$= \frac{1}{36 \pi \times 10^9} = 8.849 \times 10^{-12} \text{ F/m}$$

and ε_r = relative permittivity of the semiconductor

= 16 for germanium

= 12 for silicon

Note : In Poisson's equation, the concentration of lightly doped side is used. If we assume that n-type is lightly doped compared to p-type then as N_D less than N_A, Poisson's equation modifies to,

$$\frac{d^2 V}{d x^2} = \frac{q N_D}{\varepsilon}$$

Integrating equation (2.36) w.r.t. x we get,

$$\int \frac{d^2 V}{d x^2} dx = \int \frac{q N_A}{\varepsilon} dx$$

$$\therefore \quad \frac{dV}{dx} = \frac{q N_A x}{\varepsilon} \quad \text{... (2.38)}$$

Assume constant of integration as zero.

Now $\frac{dV}{dx}$ is the electric field intensity over the region 0 to W over which depletion region is spreaded.

$$\therefore \quad E = \frac{q N_A x}{\varepsilon} \quad \text{... (2.39)}$$

where E is electric field intensity.

To get the potential, integrating equation (2.38) we get,

$$\int \frac{dV}{dx} dx = \int_0^W \frac{q N_A}{\varepsilon} x \, d x$$

$$\therefore \quad V = \frac{q N_A}{\varepsilon} \frac{W^2}{2} \quad \text{... (2.40)}$$

At x = W, V = V_B which is barrier potential

Now barrier potential is the difference between internally developed junction potential and externally applied bias voltage.

$$\therefore \quad V_B = V_J - V \quad \text{... (2.41)}$$

where V_B is barrier potential and V must be taken as negative for reverse bias.

Substituting in equation (2.40) we get,

$$V_B = \frac{q N_A}{\varepsilon} \frac{W^2}{2} \quad \text{... (2.42)}$$

From the above equation it can be observed that ,

$$W \propto \sqrt{V_B} \quad \text{... (2.43)}$$

The width of barrier i.e. depletion layer increases with applied reverse bias.

If A is the area of cross-section of the junction, then net charge Q in the distance W is

$$Q = \text{Number of charged particle} \times \text{charge on each particle}$$

$$\therefore \quad Q = [N_A \times \text{Volume}] \times q$$

$$\therefore \quad Q = N_A A W q \quad \text{... (2.44)}$$

Now differentiating equation (2.42) with respect to V,

$$1 = \frac{1}{2}\frac{N_A q}{\varepsilon}\left[\frac{dW}{dV}\right].2W \quad \text{... (2.45)}$$

$$\therefore \quad \frac{dW}{dV} = \frac{\varepsilon}{q N_A W} \quad \text{... (2.46)}$$

Now differentiating equation (2.44),

$$\frac{dQ}{dV} = N_A A q \frac{dW}{dV}$$

$$= N_A A q . \frac{\varepsilon}{q N_A W}$$

$$\therefore \quad \frac{dQ}{dV} = \frac{\varepsilon A}{W} \quad \text{... (2.47)}$$

But $\frac{dQ}{dV}$ is the transition capacitance C_T hence

$$C_T = \frac{\varepsilon A}{W} \quad \text{... (2.48)}$$

Now from equation (2.41) we know that $V_B = V_J - V$ and for reverse bias V is negative. Hence for reverse biased condition we get $V_B = V_J + V$ where V is applied reverse biased voltage. So as reverse biased voltage increases, V_B increases. From equation (2.43), we can conclude that the width of depletion layer increases as reverse bias increases. Increasing width W, decreases the transition capacitance C_T. Hence transition capacitance C_T decreases as the reverse bias voltage increases.

$$C_T \propto \frac{1}{W} \quad \text{... (2.49)}$$

Hence the variation of C_T with respect to applied reverse biased voltage can be shown as in Fig. 2.16.

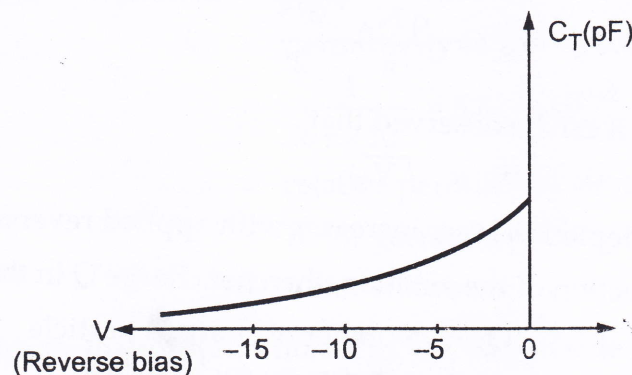


Fig. 2.16 C_T against reverse biased voltage

5) (a) Zener diode as a voltage Regulator

[circuit: V_{in}, resistor R with current I, zener diode with V_2 and I_2, load R_L with I_L]

from given fig $I = \frac{V_{in} - V_2}{R}$

$I = I_L + I_2$

Case I: Regulation with varying I/P voltage & fixed R_L

As V_{in} increases, I increases. But since R_L is fixed so I_L will be fixed, hence maximum current passes through zener diode ie I_2 increases & V_{out} remains constant as $V_{out} = \frac{I_L}{R}$ (both are constant)

As V_{in} decreases, so I_2 decreases but I_L is constant but I_2 should be hight enough to operate zener in breakdown region.

Case II:- With varying R_L & constant V_{in}

As V_{in} is constant, I is constant

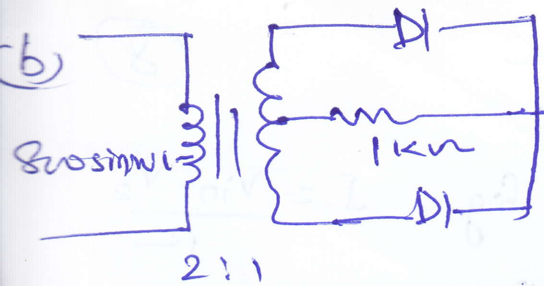
So if we increase R_L, I_L will decrease ie I_2 will increase, so zener goes in breakdown maintaining constant V_2. hence V_{out}

If R_L is decrease, I_L will increase, ie I_2 will decrease, but operating zener in breakdown maintaining const V_{out}

As $V_{out} = V_{in} - IR$

V_{in} ↓ const, IR ↓ const.

b)



V_1 (voltage at primary) is $800 \sin \omega t$

V_2 (voltage at secondary)

Given :- $\frac{N_1}{N_2} = 2 : 1$

$\frac{V_1}{V_2} = \frac{N_1}{N_2} \Rightarrow V_2 = \frac{800}{2} = 400$

$V_m = 400$

$I_m = \frac{E_m}{R_f + R_L} = \frac{400}{1000 + 10} = \frac{40}{101}$

$I_{dc} \Rightarrow \frac{2 I_m}{\pi} = \frac{2 \times 40}{101 \times \pi} = 0.25 A$

$I_{rms} \Rightarrow \frac{I_m}{\sqrt{2}} = 0.28 A$

Ripple factor $= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = 50\%$

efficiency $= \frac{P_{dc}}{P_{ac}} = \frac{I^2_{dc} R_L}{I_2^2{}_{rms}(R_f + R_L)}$

$\Rightarrow \frac{(0.25)^2 \times 1000}{(0.28)^2 \times 1010}$

$\Rightarrow .789 \simeq 80\%$

3.13 The Semiconductor Photodiode

If a reverse-biased *p-n* junction is illuminated, the current varies almost linearly with the light flux. This effect is exploited in the semiconductor *photodiode*. This device consists of a *p-n* junction embedded in a clear plastic, as indicated in Fig. 3.20. Radiation is allowed to fall upon one surface across the junction. The remaining sides of the plastic are either painted black or enclosed in a metallic case. The entire unit is extremely small and has dimensions of the order of tenths of an inch.

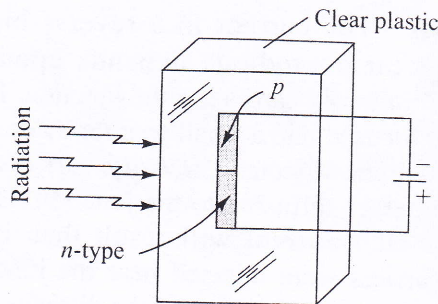


Fig. 3.20 *The construction of a semiconductor photodiode.*

Volt-Ampere Characteristics If reverse voltages in excess of a few tenths of a volt are applied, an almost constant current (independent of the magnitude of the reverse bias) is obtained. The dark current corresponds to the reverse saturation current due to the thermally generated minority carriers. As explained in Sec. 3.2, these minority carriers "fall down" the potential hill at the junction, whereas this barrier does not allow majority carriers to cross the junction. Now if light falls upon the surface, additional electron-hole pairs are formed. In Sec. 2.8 we note that it is justifiable to consider the radiation solely as a *minority-carrier injector.* These injected minority carriers (for example, electrons in the *p* side) diffuse to the junction, cross it, and contribute to the current.

The reverse saturation current I_o in a *p-n* diode is proportional to the concentrations p_{no} and n_{po} of minority carriers in the *n* and *p* region, respectively. If we illuminate a reverse-biased *p-n* junction, the number of new hole-electron pairs is proportional to the number of incident photons. Hence the current under large reverse bias is $I = I_o + I_s$, where I_s, the short-circuit current, is proportional to the light intensity. Hence the volt-ampere characteristic is given by

$$I = I_s + I_o(1 - e^{V/\eta V_T})x \tag{3.34}$$

where I, I_s and I_o represent the *magnitude* of the reverse current, and V is positive for a forward voltage and negative for a reverse bias. The parameter η is unity for germanium and 2 for silicon, and V_T is the volt equivalent of temperature defined by Eq. (3.10).

Typical photodiode volt-ampere characteristics are indicated in Fig. 3.21. The curves (with the exception of the dark-current curve) do not pass through the origin. The characteristics in the millivolt range and for positive bias are discussed in the following section, where we find that the photodiode may be used under either short-circuit or open-circuit conditions. It should be noted that the characteristics drift somewhat with age. The barrier capacitance $C_T \approx 10$ pF, the dynamic resistance $R \approx 50$ M, and the ohmic resistance $r \approx 100\ \Omega$.

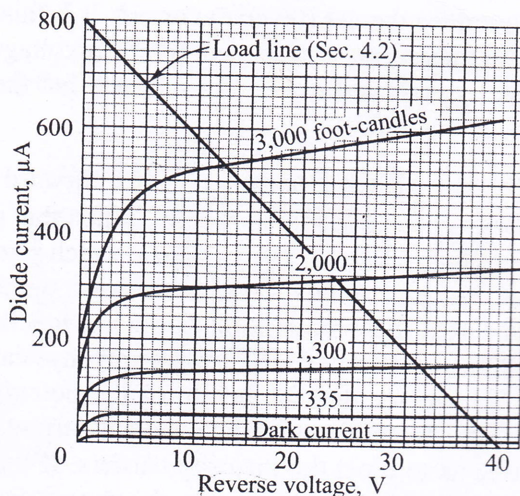


Fig. 3.21 *Volt-ampere characteristics for the 1N77 germanium photodiode. (Courtesy of Sylvania Electric Products, Inc.)*

Sensitivity with Position of Illumination The current in a reverse-biased semiconductor photodiode depends upon the diffusion of minority carriers to the junction. If the radiation is focused into a small spot far away from the junction, the injected minority carriers can recombine before diffusing to the junction. Hence a much smaller current will result than if the minority carriers were injected near the junction. The photocurrent as a function of the distance from the junction at which the light spot is focused is indicated in Fig. 3.22. The curve is somewhat asymmetrical because of the differences in the diffusion lengths of minority carriers in the *p* and *n* sides. Incidentally, the spectral response of the semiconductor photodiode is the same as that for a photoconductive cell, and is indicated in Fig. 2.12.

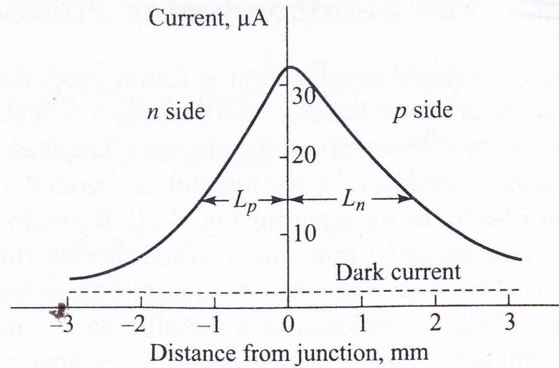


Fig. 3.22 *Sensitivity of a semiconductor photodiode as a function of the distance of the light spot from the junction.*

The *p-n* photodiode and, particularly, the improved *n-p-n* version described in Sec. 5.14 find extensive application in light-detection systems, reading of film sound track, light-operated switches, production-line counting of objects which interrupt a light beam, optical communication receivers, etc.

3.14 The Photovoltaic Effect[8]

In Fig. 3.21 we see that an almost constant reverse current due to injected minority carriers is collected in the *p-n* photodiode for large reverse voltages. If the applied voltage is reduced in magnitude, the barrier at the junction is reduced. This decrease in the potential hill does not affect the minority current (since these particles fall down the barrier), but when the hill is reduced sufficiently, some majority carriers can also cross the junction. These carriers correspond to a forward current, and hence such a flow will reduce the net (reverse) current. It is this increase in majority-carrier flow which accounts for the drop in the reverse current near the zero-voltage axis in Fig. 3.21. An expanded view of the origin in this figure is indicated in Fig. 3.23. (Note that the first quadrant of Fig. 3.21 corresponds to the third quadrant of Fig. 3.23.)

The Photovoltaic Potential If a forward bias is applied, the potential barrier is lowered, and the majority current increases rapidly. When this majority current equals the minority current, the total current is reduced to zero. The voltage at which zero resultant current is obtained is called the *photovoltaic* potential. Since, certainly, no current flows under open-circuited conditions, the photovoltaic emf is obtained across the open terminals of a *p-n* junction.

An alternative (but of course equivalent) physical explanation of the photovoltaic effect is the following: In Sec. 3.1 we see that the height of the potential barrier at an open-circuited (nonilluminated) *p-n* junction adjusts itself so that the resultant current is zero, the electric field at the junction being in such a direction as to repel the majority carriers. If light falls on the surface, minority carriers are injected, and since these fall down the barrier, the minority current increases. Since under open-circuited conditions the total current must remain zero, the majority current (for example, the hole current in the *p* side) must increase the same amount as the minority current. This rise in majority current is possible only if the retarding field at the junction is reduced. Hence the barrier height is automatically lowered as a result of the radiation. Across the diode terminals there appears a voltage just equal to the amount by which the

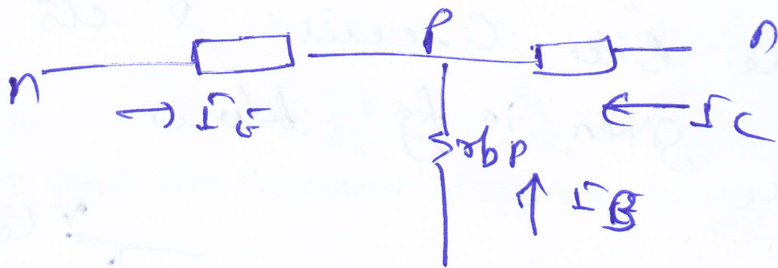
The Ebers-Moll model

The transistor current is given by the equation

$$I_C = \alpha I_E + I_{CO}$$

Where I_E is emitter current, α is gain of current and I_{CO} is leakage current due to minority carrier or in terms of p-n junction it is reverse saturation current flowing from N to P

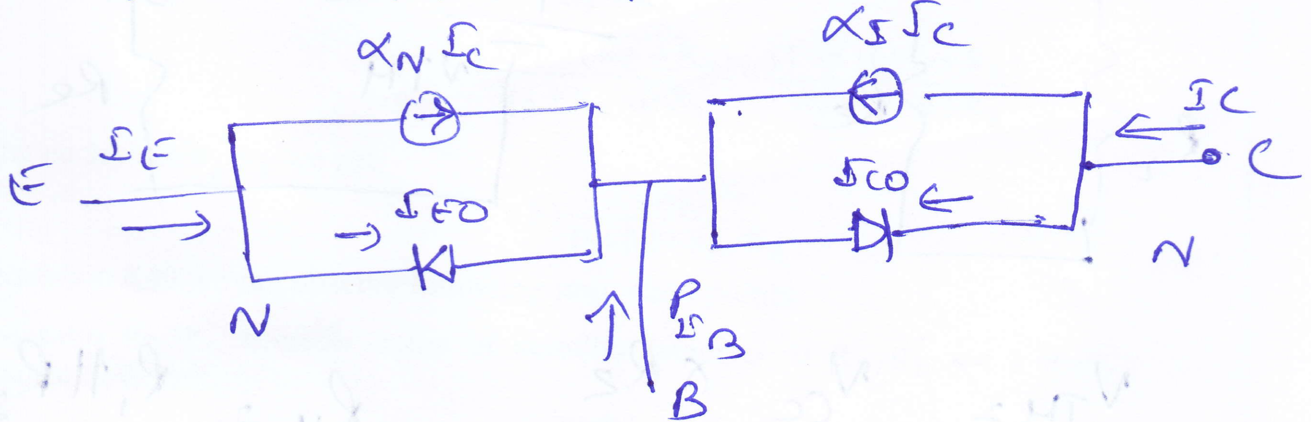
So for n-p-n transistor



$$I_C = \alpha I_E + I_0(e^{V_C/V_T} - 1)$$

$$\text{or } \alpha_N I_E + I_0(e^{V_C/V_T} - 1)$$

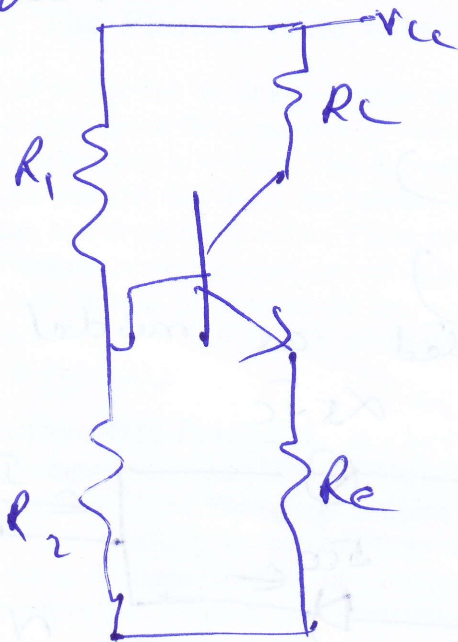
This equation can be represented as model

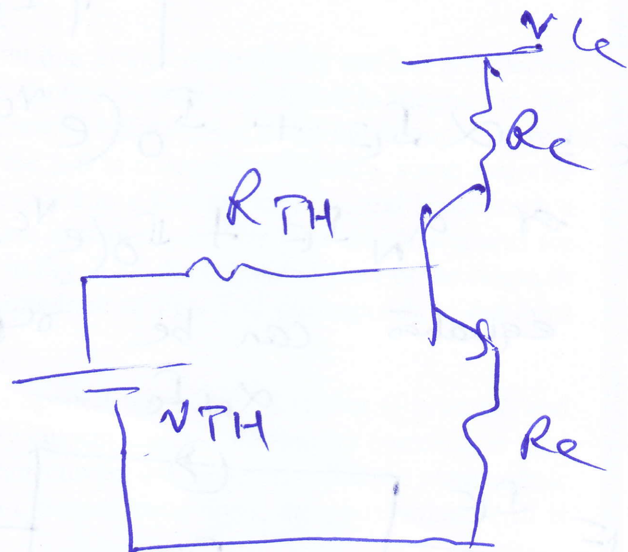


in this mode two diodes are connected back to back ie PN & NP or NP & PN forming PNP or NPN with two current controlled current source. representing as a leakage

This model is valid for both reverse & forward state voltage applied across transistor junction. This model shows why it is impossible to construct a transistor by simply connecting two seperate diode in series opposing, because if the current source are eliminated, all minority carrier will recombine in the base & none will survive to reach the collector.

(b) Voltage divider bias circuit & its equivalent is given in fig below





$$V_{TH} = \frac{V_{CC} \times R_2}{R_1 + R_2}, \quad R_{TH} = R_1 \parallel R_2$$

Here Thevenin's equivalent voltage V_T is given by

$$V_T = \frac{R_2 \times V_{CC}}{R_1 + R_2} \text{ and}$$

the R_1 and R_2 are replaced by R_B which is the parallel combination of R_1 and R_2.

$$\therefore \quad R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Applying KVL to the base circuit we get,

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

Differentiating w.r.t. I_C and considering V_{BE} to be independent of I_C we get,

$$0 = \frac{\partial I_B}{\partial I_C} \times R_B + \frac{\partial I_B}{\partial I_C} \times R_E + R_E$$

$$\therefore \quad \frac{\partial I_B}{\partial I_C}(R_E + R_B) = -R_E$$

$$\therefore \quad \frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_E + R_B} \quad \ldots (6.38)$$

We have already seen the generalized expression for stability factor S given by equation 6.9 is

$$S = \frac{1+\beta}{1-\beta(\partial I_B / \partial I_C)} \quad \ldots (6.39)$$

Substituting value of $\frac{\partial I_B}{\partial I_C}$ in the equation 6.39 we get,

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E + R_B}\right)}$$

$$S = \frac{(1+\beta)(R_E + R_B)}{R_B + R_E + \beta R_E} = \frac{(1+\beta)(R_E + R_B)}{R_B + (1+\beta) R_E}$$

Dividing each term by R_E we get,

$$S = (1+\beta) \frac{1 + R_B/R_E}{(1+\beta) + R_B/R_E} \quad \ldots (6.40)$$

From equation 6.40 we can observe following important points

1. The ratio R_B/R_E controls value of stability factor S. If $R_B/R_E \ll 1$ then equation 6.40 reduces to

$$S = (1+\beta) \cdot \frac{1}{(1+\beta)} = 1 \quad \ldots (6.41)$$

Practically $R_B/R_E \neq 0$. But to have better stability factor S we have to keep ratio R_B/R_E as small as possible.

2. To keep R_B/R_E small, it is necessary to keep R_B small. This means that $R_1 || R_2$ must be small. Due to small value of R_1 and R_2, potential divider circuit will draw more current from V_{CC} reducing the life of the battery. So while designing if we make R_2 much smaller than R_1 then parallel combination results small R_B without drawing more current through V_{CC}. Another important aspect is that reducing R_B will reduce input impedance of the circuit, since R_B comes in parallel with the input. This reduction of input impedance in amplifier circuits is not desirable and hence R_B cannot be made very small.
3. Emitter resistance R_E is the another parameter we can use to decrease ratio R_B/R_E. By increasing R_E we can make R_B/R_E small. But as we increase R_E, drop $I_E R_E$ will also increase and since V_{CC} is constant, drop across R_C will reduce. This shifts the operating point Q which is not desirable and hence there is limit for increasing R_E.

Thus while designing voltage divider bias circuit we have to find compromising values :

S – Small

R_B – Reasonably small

R_E – not very large

4. If ratio R_B/R_E is fixed, S increases with β. Therefore stability decreases with increasing β.
5. Stability factor S is essentially independent of β for small value of S.

Note : Stability factor S for voltage divider bias or self bias is less as compare to other biasing circuits studied. So this circuit is most commonly used.

Ex. 6.7 : *For a circuit shown in Fig. 6.27,* $V_{CC} = 20\ V$, $R_C = 2\ k\Omega$, $\beta = 50$, $V_{BEact} = 0.2V$, $R_1 = 100\ k\Omega$, $R_2 = 5k\Omega$ *and* $R_E = 100\Omega$. *Calculate* I_B, V_{CE}, I_C *and stability factor S.*

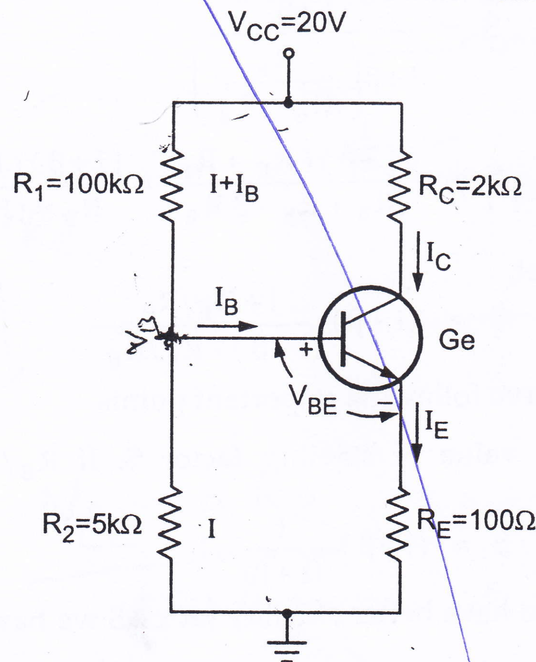


Fig. 6.27

in the collector current. The process is cumulative and it is referred to as **self heating**. The excess heat produced at the collector base junction may even burn and destroy the transistor. This situation is called '**Thermal runaway**' of the transistor.

6.8.1 Thermal Resistance

The steady state temperature rise at the collector junction is proportional to the power dissipated at the junction. It is given as

$$\partial T = T_j - T_A = \theta P_D \quad \text{... (6.63)}$$

where T_j = Junction temperature in °C.

T_A = Ambient temperature in °C.

and P_D = Power in watts dissipated at the collector junction.

θ = Constant of proportionality.

The θ, which is constant of proportionality is referred to as thermal resistance.

$$\theta = \frac{T_j - T_A}{P_D} \quad \text{... (6.64)}$$

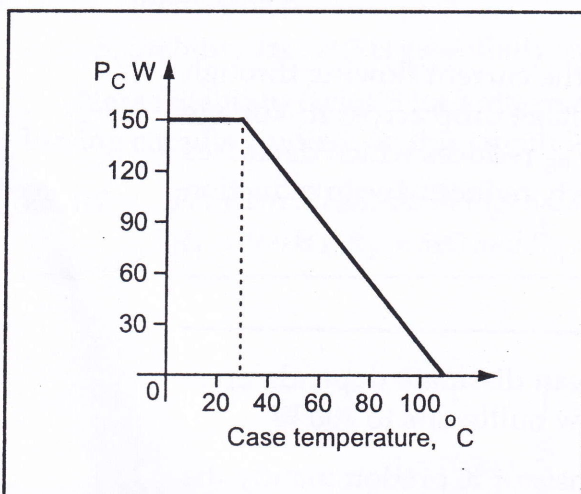


Fig. 6.43 Power temperature derating curve

The unit of θ, the thermal resistance, is °C/watt. The typical values of θ for various transistors vary from 0.2 °C/W for a high power transistor with an efficient heat sink to 1000 °C/W for a low power transistor. The maximum collector power P_C allowed for safe operation is specified at 25 °C.

Fig. 6.43 shows power-temperature derating curve for a germanium transistor.

It shows that above 25 °C, collector power must be decreased, and at the extreme temperature at which the transistor may operate, P_C is reduced to zero.

6.8.2 The Condition for Thermal Stability

As we know, the thermal runaway may even burn and destroy the transistor, it is necessary to avoid thermal runaway. The required condition to avoid thermal runaway is that the rate at which heat is released at the collector junction must not exceed the rate at which the heat can be dissipated. It is given by,

$$\frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_j} \quad \text{... (6.65)}$$

It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate-source voltage i.e.

$$\text{a.c. drain resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}$$

For instance, if a change in drain voltage of 2 V produces a change in drain current of 0.02 mA, then,

$$\text{a.c. drain resistance, } r_d = \frac{2\text{ V}}{0.02\text{ mA}} = 100\text{ k}\Omega$$

Referring to the output characteristics of a *JFET* in Fig. 19.8, it is clear that above the pinch off voltage, the change in I_D is small for a change in V_{DS} because the curve is almost flat. Therefore, drain resistance of a *JFET* has a large value, ranging from 10 kΩ to 1 MΩ.

(*ii*) **Transconductance (g_{fs}).** The control that the gate voltage has over the drain current is measured by transconductance g_{fs} and is similar to the transconductance g_m of the tube. It may be defined as follows :

It is the ratio of change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) at constant drain-source voltage i.e.

$$\text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}$$

The transconductance of a *JFET* is usually expressed either in mA/volt or micromho. As an example, if a change in gate voltage of 0.1 V causes a change in drain current of 0.3 mA, then,

$$\text{Transconductance, } g_{fs} = \frac{0.3\text{ mA}}{0.1\text{ V}} = 3\text{ mA/V} = 3 \times 10^{-3}\text{ A/V or mho or } S \text{ (siemens)}$$

$$= 3 \times 10^{-3} \times 10^{6}\ \mu\text{ mho} = 3000\ \mu\text{ mho (or } \mu\text{S)}$$

(*iii*) **Amplification factor (μ).** *It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in gate-source voltage (ΔV_{GS}) at constant drain current i.e.*

$$\text{Amplification factor, } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D$$

Amplification factor of a *JFET* indicates how much more control the gate voltage has over drain current than has the drain voltage. For instance, if the amplification factor of a *JFET* is 50, it means that gate voltage is 50 times as effective as the drain voltage in controlling the drain current.

19.14 Relation Among JFET Parameters

The relationship among *JFET* parameters can be established as under :

$$\text{We know} \quad \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

Multiplying the numerator and denominator on R.H.S. by ΔI_D, we get,

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\therefore \quad \mu = r_d \times g_{fs}$$

i.e. amplification factor = a.c. drain resistance × transconductance

Example 19.7. *When a reverse gate voltage of 15 V is applied to a JFET, the gate current is 10^{-3} μA. Find the resistance between gate and source.*

Solution. $V_{GS} = 15\text{ V}\ ;\ I_G = 10^{-3}\ \mu\text{A} = 10^{-9}\text{ A}$

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$$= 3 \times 10^{-3} \times 10^{6}\ \mu\text{ mho} = 3000\ \mu\text{ mho (or } \mu\text{S)}$$

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$$\therefore \quad \mu = r_d \times g_{fs}$$

i.e. amplification factor = a.c. drain resistance × transconductance

Example 19.7. *When a reverse gate voltage of 15 V is applied to a JFET, the gate current is 10^{-3} μA. Find the resistance between gate and source.*

Solution. $V_{GS} = 15\text{ V}$; $I_G = 10^{-3}\ \mu\text{A} = 10^{-9}\text{ A}$

Like, depletion type MOSFET, two highly doped n regions are diffused into a lightly doped p type substrate. The source and drain are taken out through metallic contacts to n-doped regions as shown in the Fig. 8.19. But the channel between two n-regions is absent in the enhancement type MOSFET. The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material.

b) Basic Operation and Characteristics :

On application of drain to source voltage V_{DS} and keeping gate to source voltage zero by directly connecting gate terminal to the source terminal, practically zero current flows-quite different from the depletion type MOSFET and JFET. If we increase magnitude of V_{GS} in the positive direction the concentration of electrons near the SiO_2 surface increases. At particular value of V_{GS} there is a measurable current flow between drain and source. This value of V_{GS} is called threshold voltage denoted by V_T. Thus we can say that in an enhancement type n-channel MOSFET, a positive gate voltage above a threshold value induces a channel and hence the drain current by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer, as shown in the Fig. 8.20. The conductivity of the channel is enhanced by increasing the gate to source voltage and thus pulling more electrons into the channel. For any voltage below the threshold value, there is no channel.

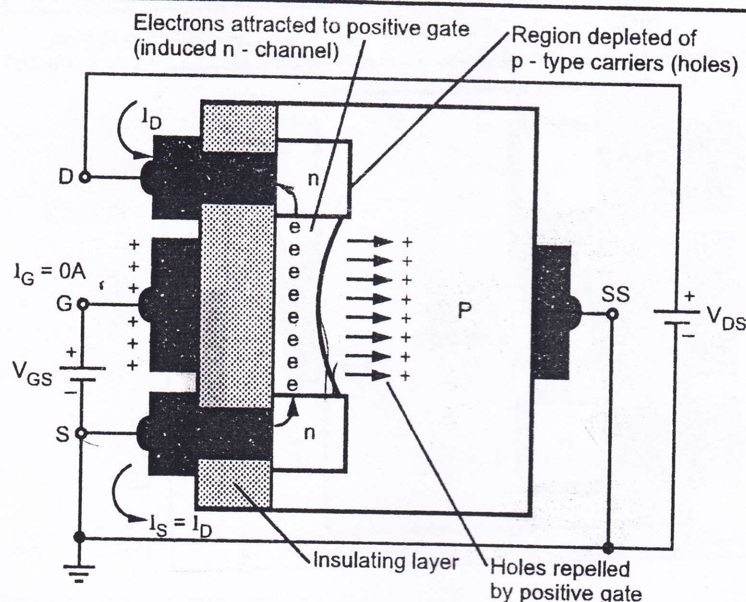


Fig. 8.20 Channel formation in the n-channel enhancement type MOSFET

Since the channel does not exist with $V_{GS} = 0V$ and "enhanced" by the application of a positive gate to source voltage, this type of MOSFET is called an enhancement type MOSFET.

Fig. 8.21 shows the drain characteristics of an n-channel enhancement type MOSFET. Looking at Fig. 8.21 we can say that as V_{GS} increases beyond the threshold level, the density of free carriers (electrons) in the induced channel increases, increasing the drain

current. However, at some point of V_{DS}, for constant V_{GS}, the drain current reaches a saturation level. The levelling off of I_D is due to a pinch-off process, is as described earlier for the JFET. Fig. 8.22 shows pinch off process for n-channel enhancement type MOSFET.

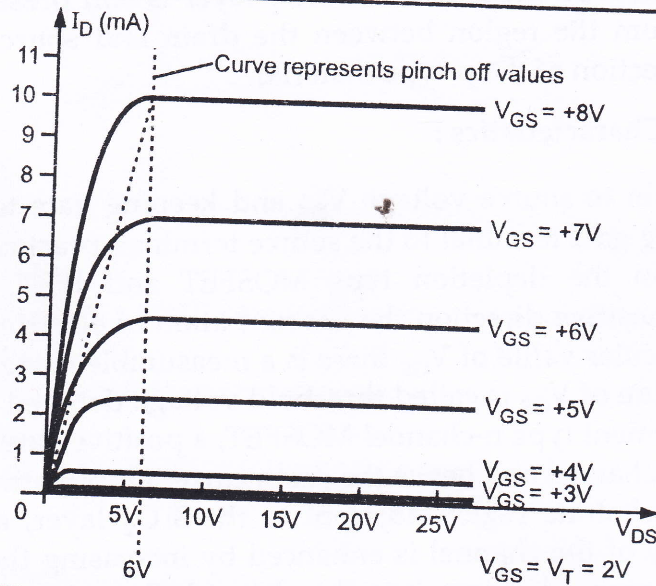


Fig. 8.21 Drain characteristics of an n-channel enhancement type MOSFET

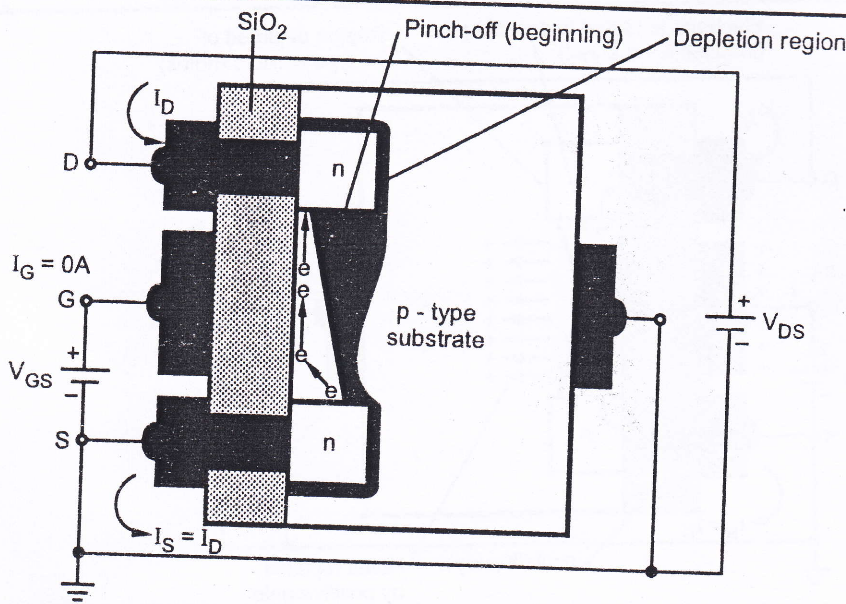
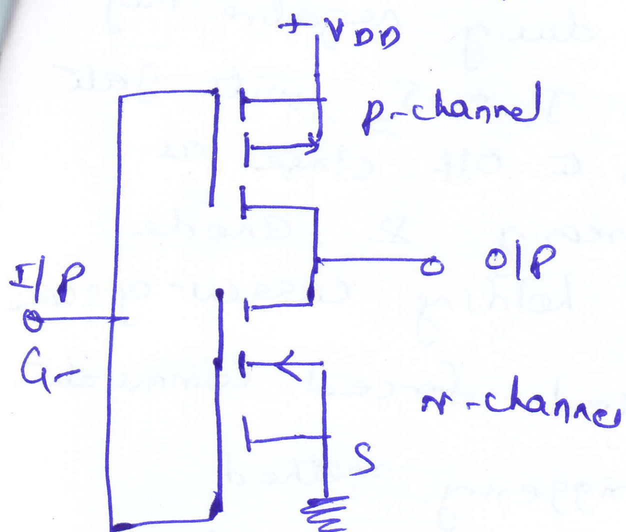


Fig. 8.22 Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS}

Fig. 8.23 shows the transfer characteristic for n-channel enhancement type MOSFET. This characteristic is quite different from characteristic that we obtained for JFET and depletion type MOSFET. For an n-channel enhancement type MOSFET it is now totally in the positive V_{GS} region and as we know I_D does not flow until $V_{GS} = V_T$.

(c) CMOS as an inverter

In CMOS logic both P-type & N-type MOS transistors are used in same chip. The circuit diagram is shown below



In fig. P-channel device is connected to +VDD & the source of N-channel is grounded. Here +VDD represent logic 1 & 0 will represent logic 0.

When input is near ground level, the gate to source in P-channel transistor is of the order of supply voltage VDD, hence it gets turned ON. A low resistance path is created between the supply voltage & O/P. On the other hand high resistance path is established between O/P and ground. As a result N-channel FET is off. The O/P will be same as supply voltage +VDD. When the inverter input is high at +VDD, N-channel is ON & P-channel is off. The operation in this state is exactly the inverse of that described when input is low. In this way we get O/P as grounded level as P-channel is off & circuit consumes no power except leakage current.

Q.6) (a) Two techniques for turning SCR-off

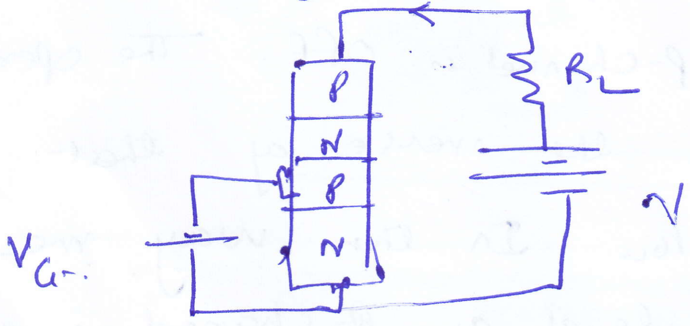
(i) Natural (ii) forced

In natural, we apply a-c voltage to SCR, instead of d-c which make anode-cathode R.B during negative half cycle, thus reverse biasing Junction J_1 & J_3, with gate open. After some time SCR goes to off stage as its forward current starts decreasing & anode current goes below the rating holding current of SCR

(ii) forced :- This is also called forced commutation

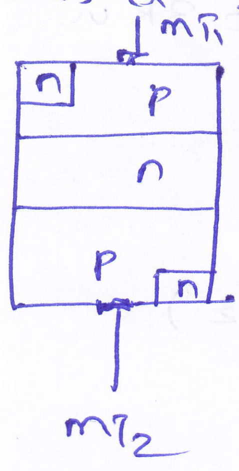
one of this method is gate triggering method

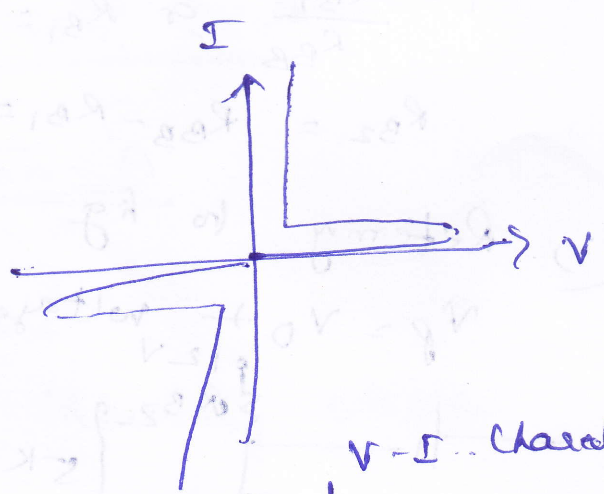
In this we apply a -ve pulse to gate, instead of a short +ve pulse. This will make J_2 reverse bias thus will not allow the charge carrier to move from anode to cathode. After some time due to R.B on gate when depletion region of J_2 increases that charges moving from anode to cathode gets recombined in this region ~~& get~~ lost making SCR off

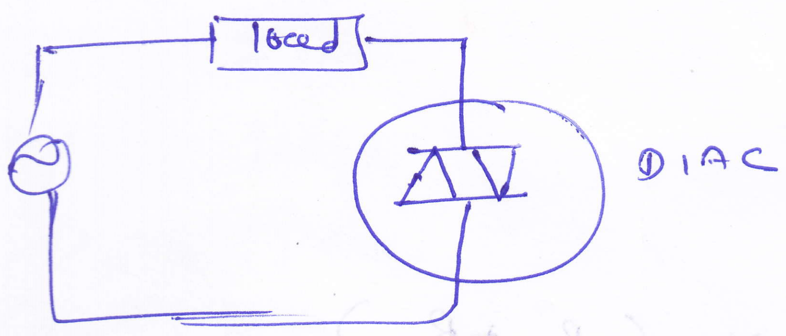


Working of DIAC

It is a two terminal bidirectional switching device







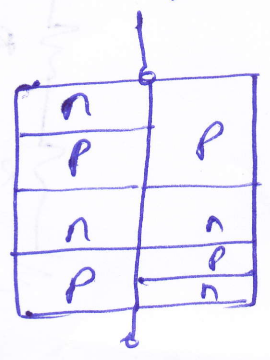


fig (i)

As shown in fig (i) during positive half cycle, the right four layer diode conducts heavily only when the supply voltage exceeds the breakdown voltage of the diac. In this case, right latch closes. On the other hand during -ve half cycle, left diode conducts heavily when supply voltage exceeds breakdown voltage. Once diac starts conducting, it stops only when current flowing through diac reduces below the rated holding current of diac. The wave shape of o/p voltage across load is also shown in fig.

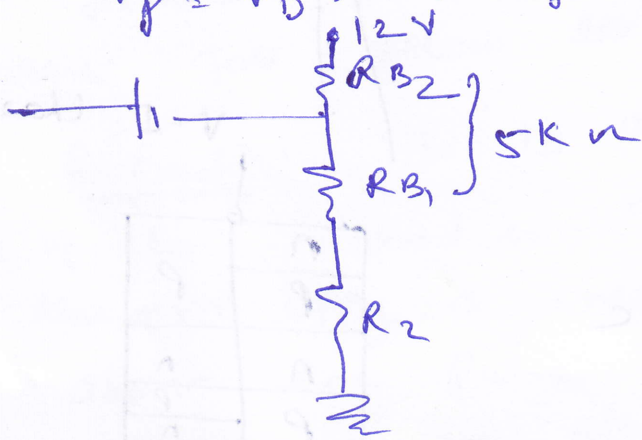
Q6) (c) Given $V_S = 12$, $R_{BB} = 5K\Omega$, $\eta = 0.6$

$\eta = \frac{R_{B1}}{R_{BB}}$ or $R_{B1} = \eta R_{BB} = 0.6 \times 5 k\Omega = 3k\Omega$

$R_{B2} = R_{BB} - R_{B1} = 5 - 3 = 2 k\Omega$

(ii) Referring to fig

$V_P = V_D +$ voltage drop across $(R_{B1} + R_2)$



$\Rightarrow 0.7 + \frac{V_S (R_{B1} + R_2)}{R_{BB} + R_2}$

$\Rightarrow 0.7 + \frac{12V}{5K + 0.1K} \times (3 + 0.1) K$

$= 8V$

(iii) $t = R_1 C \log_e \frac{1}{1-\eta}$

Here $R_1 = 50K\Omega$, $C = 0.1 \times 10^{-12}$

$t = 50 \times 10^{3} \times 0.1 \times 10^{-12} \log_e \frac{1}{1-0.6}$

$\Rightarrow 4.58\,\mu s$

$f = \frac{1}{t} = \frac{1}{4.58 \times 10^{-6}} = 218 KHz$